REMARKS

Claims 1-13 are pending in this application.

Claims 10-13 are rejected under 35 U.S.C. §102(b) as being anticipated by Iwazaki, US 6,073,244. This rejection is respectfully traversed.

Claims 1-5, and 7-10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Iwazaki. This rejection is respectfully traversed.

Claim 6 is rejected under 35 U.S.C. §103(a) as being unpatentable over Iwazaki and further in view of O'Brien, US 5,596,756. This rejection is respectfully traversed.

Claim Rejections

Applicant has reviewed the outstanding office action and thought the present invention is patenatably distinguishable over the reference to Iwazati. Applicant respectfully requests that the Examiner withdraw the claim rejections because of the following statements.

Applicant notes the objective of the present invention is to provide a real-time monitor and to adjust the operating rate of each device fabricated on the motherboard for redeploying the whole system source to obtain the most efficient performance of the motherboard. That is why in the present invention, each device, such as the CPU 12, the north bridge chip 14, the south bridge chip 16, the AGP slot 20, the PCI slot 22 and the power supply 24, is monitored by the individual performance monitor means 26, and those devices are separately connected to the performance control chip 28 for acquiring the specific control signal individually.

It is clearly recited in the paragraph [0017] of the present invention as:

"As to the performance control chip 28 is **connected separately to each device** on the motherboard 10, to **compare the operating state of each device** according to the flow rate provided by the performance monitor means 26. Then, the performance control chip 28 can **redeploy the system source shared by each device, to adjust the operating rate of each device for promoting the whole system performance** of the motherboard 10."

Oppositely, in Iwazaki, the devices of the motherboard are only divided to two types, one is the CPU, the other is the peripheral processing unit. As illustrated in FIG. 5 of Iwazaki, both the peripheral processing unit 31 and 32 receive the clock signal from the clock generating

unit 1 via the signal wire 61, and the CPU 2 receives another clock signal from the clock generating unit 1A via the signal wire 62.

Besides, as shown in FIG 5 of Iwazaki, it is clearly that the bus access monitoring unit 44 is applied to monitor only the load state of the bus 5 via the signal wire 45. That means the peripheral processing units 31 and 32 are regarded as an individual relative to the CPU, and cannot be monitored or adjusted separately.

Apparently, the real-time adjusting apparatus of the present invention can optimizing the system performance more efficiently and precisely than Iwazaki, because a plurality of the performance monitor means are applied to connected separately to the corresponding one of bus lines to connect devices and further the performance control chip is connected separately to each device for adjusting the operating rate thereof.

Further, applicant wants to point out, in the present invention, the performance control chip 28 can also **send control signals to the north bridge chip 14 or the south bridge chip 16, to alter default configurations stored in the register** of the north bridge chip 14 or the south bridge chip 16, for **readjusting the priority of each device to share the system source**. Namely, in the present invention, the configurations stored in the register are dynamic to indicate the real-time priority of each device. The related description is recited clearly in the paragraph [0020] of the present invention, and cannot be found in Iwazaki. The secondary reference to O'Brien doesn't overcome the deficiencies of Iwazaki.

It is believed that the independent Claims 1, 7, and 10, are patentably distinguishable over the all citations because all these claims recite clearly the plurality of performance monitor means are introduced and the performance control chip is separately connected to each device, Applicant respectfully requests that the Examiner withdraw the claim rejections under 35 U.S.C. §103 and §102.

Summary

In view of the foregoing amendments and remarks, Applicant respectfully requests that the Examiner withdraw the rejections and expedite this application be passed to issue.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone

number listed below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

By _____

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